Side-channel Attack Standard Evaluation Board SASEBO-W Specification

Version 1.1

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National Institute of Advanced Industrial Science and Technology

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1. Overview

The SASEBO-W is a circuit board developed for side-channel attack experiments on IC Cards, a class of common cryptographic hardware. It supports power and electromagnetic analysis for ISO/IEC 7816-3 Class A/B/C contact IC Cards with corresponding measurement points. The SASEBO-W is equipped with the Xilinx FPGA Spartan-6 LX150 not only for controlling the board but also for side-channel attack experiments on the FPGA.

1.1. Features

- ISO/IEC 7816-3 Contact IC Card Support.
- Measurement points for IC Card's V_{CC} and GND.
- Measurement hole for electromagnetic analysis on the bottom side of IC Card.
- Operating on USB bus power or external input.
- Selectable IC Card voltage (1.8 V / 3.0 V / Adjustable (1.3 V ~ 4.9 V) / External).
- Automatic signal-level shifting at any IC Card power voltage.
- Selectable IC Card clock signal (via FPGA / External).
- Highly scalable Xilinx Spartan-6 series FPGA: XC6SLX150-FGG484.
- 64-bit general purpose I/O with power supply.

Table 1：Key Specifications

IC Card socket	・ISO/IEC 7816 compliant (Contact) ・Card detection ・Hole for electromagnetic measurements
IC Card voltages	・Onboard regulator 1.8 V / 3.0 V / PROG (1.3 V ~ VIN-0.1 V) ・External input 1.2 ~ 5.5 V
IC Card clock	・Supplied from FPGA ・External clock input via SMA connector
Measurement points	・High side of IC Card (V_{CC}) ・Low side of IC Card (GND) ・High side of FPGA core (V_{CORE})
FPGA	Xilinx Spartan-6 XC6SLX150-FGG484
Configuration ROM	64-Mbit SPI FLASH memory
FPGA clock	・Onboard 24-MHz oscillator ・External input via SMA connector
USB I/F	FT2232H (USB device)
General purpose LED	8 bits
General purpose switch	DIP switch 8 bits / Push button 1 bit
General purpose I/O	64 bits (2.5 V)
Rated board voltage	5 V ± 10%
Rated board current	・USB bus power : 0.75 A (Protected by resettable fuse) ・External power input : 3 A (Rated by connector)
Substrate	4 Layers, FR-4, 1.6t
Dimensions	150 mm × 200 mm

2. Board Configuration

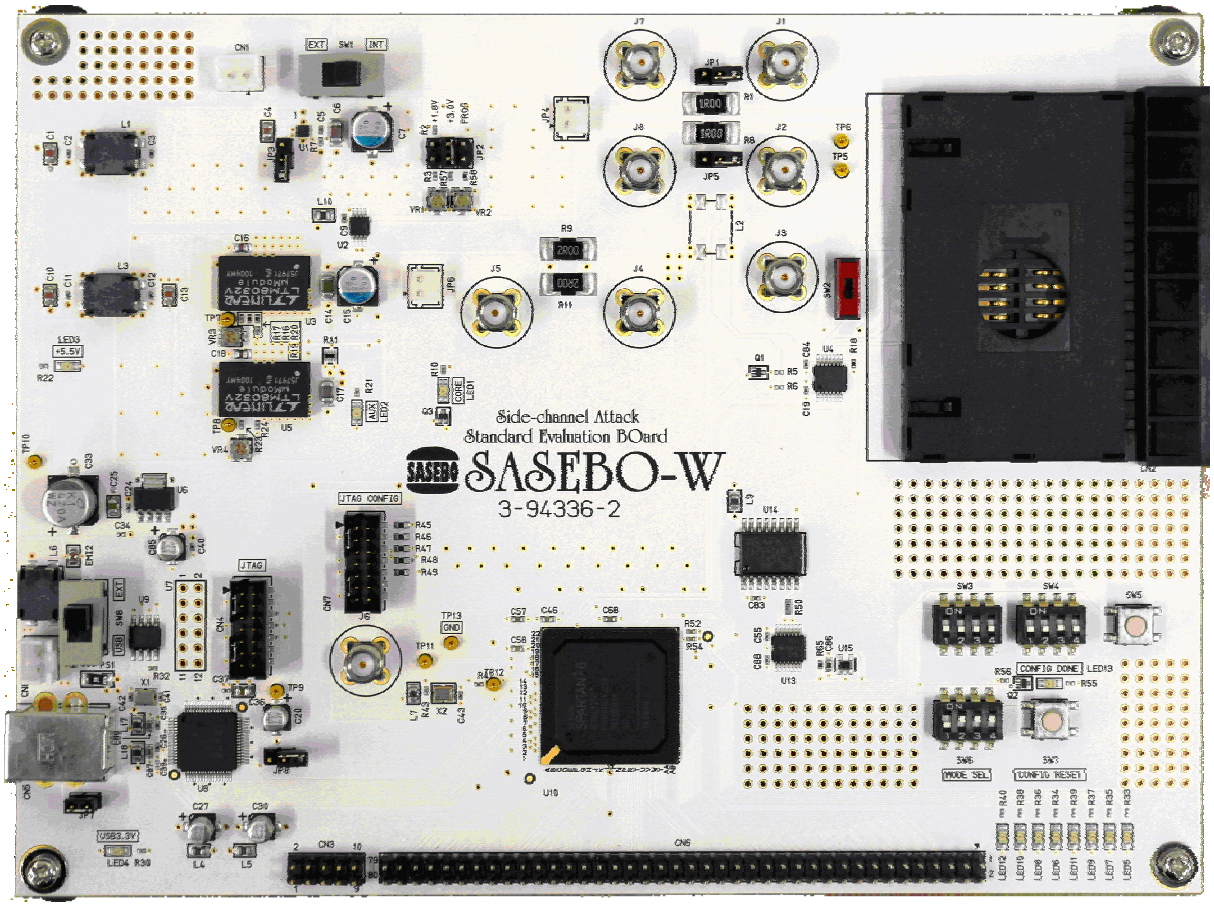

Figure 1 : SASEBO-W Top View

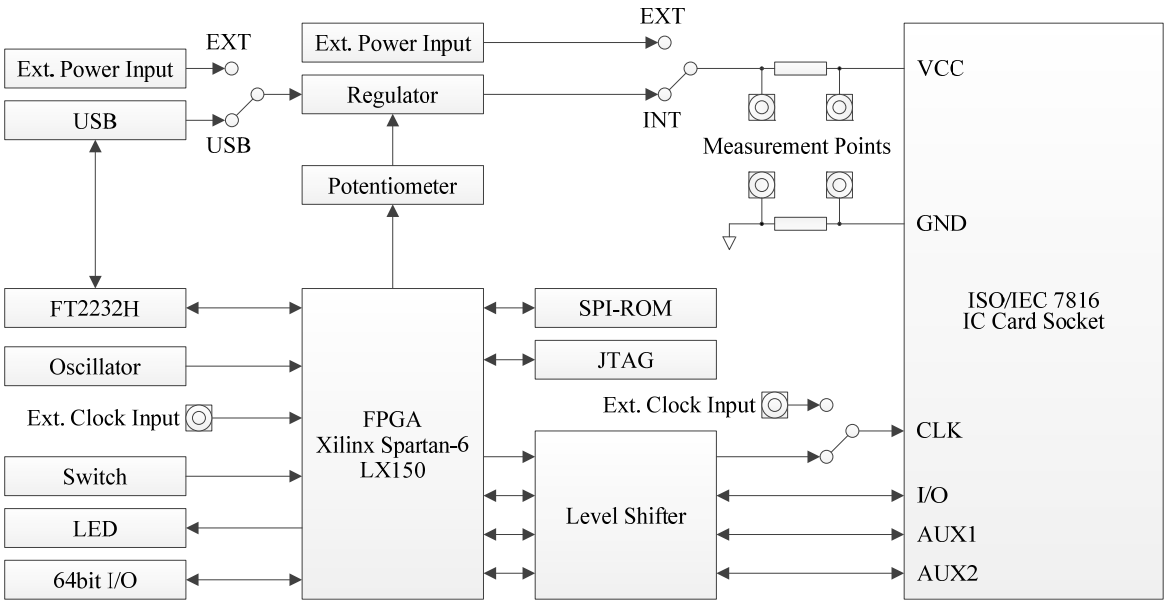

Figure 2 : SASEBO-W Block Diagram

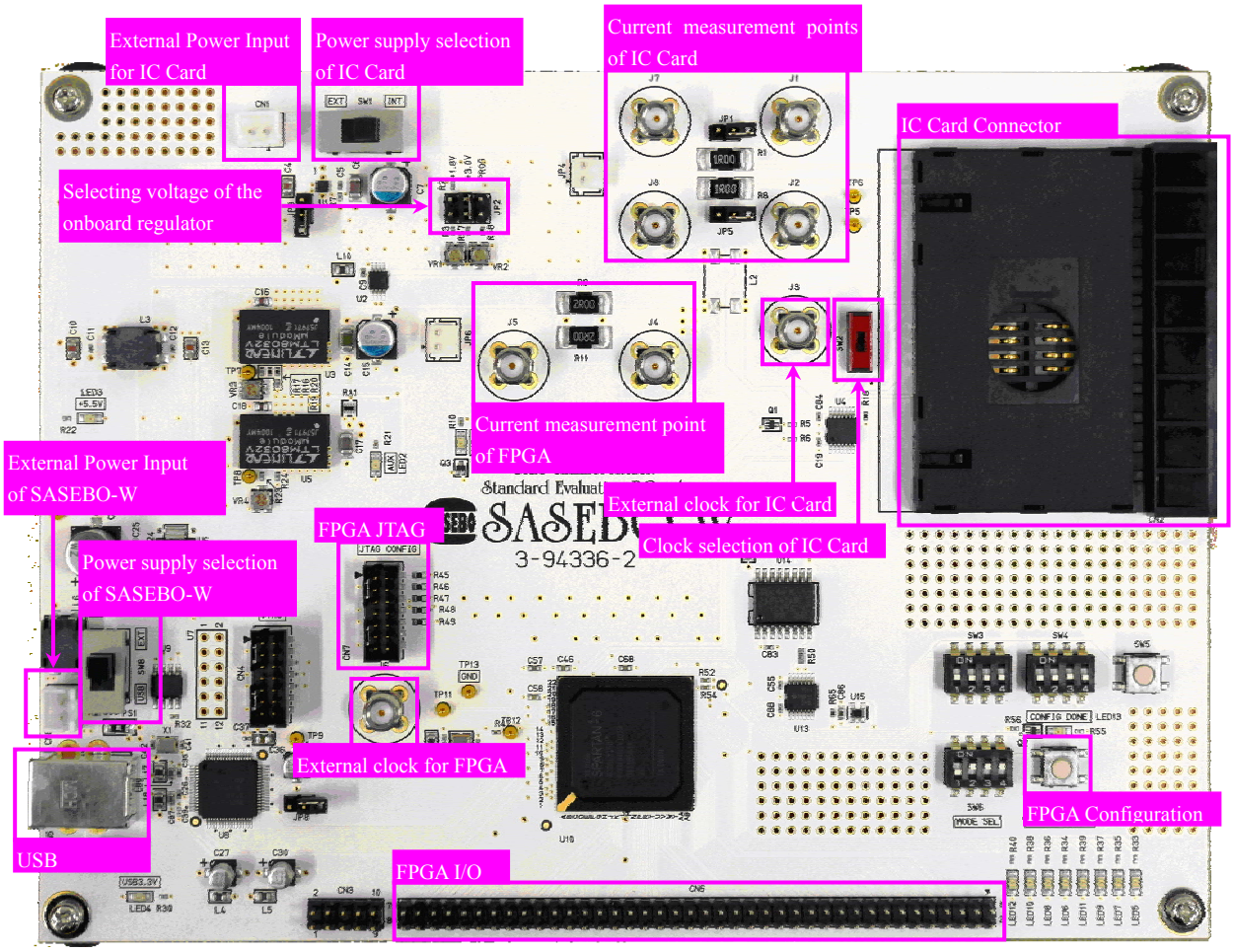

Figure 3 : SASEBO-W Board Functions

2.1. Power Circuit

The SASEBO-W is powered with 5.0 V from the USB bus (CN5) or external input (CN8) selected by SW8. The USB bus is protected by the 0.75 A resettable fuse.

The IC Card is powered from the onboard regulator IC or external input (CN1) selected by SW1. The output voltage of the onboard regulator IC is selected by JP2. The FPGA determines the voltage in the range from 1.3 V to (VIN - 0.1 V) when PROG is selected.

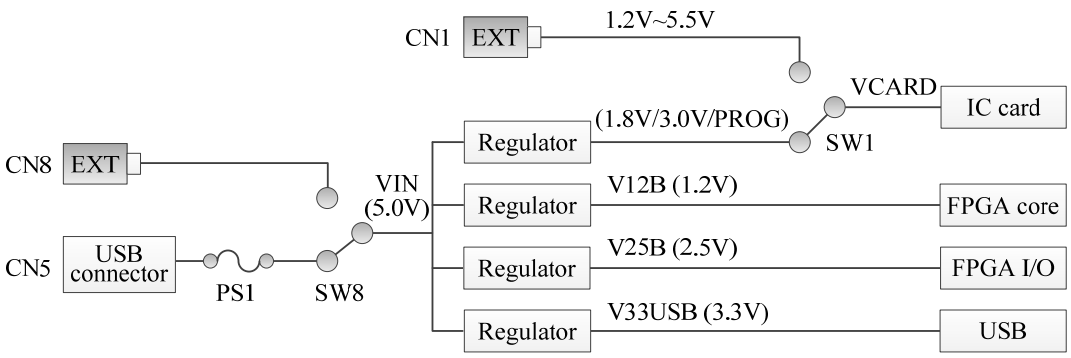

Figure 4 : Power Circuit

2.2. Voltage Calibration

The following voltages can be calibrated by trimmers.

Table 2 : Voltage Calibration Points

Trimmer	Voltage
VR1	IC Card +1.8 V (VCARD)
VR2	IC Card +3.0 V (VCARD)
VR3	FPGA core 1.2 V (V12B)
VR4	FPGA I/O 2.5 V (V25B)

2.3. Power-On Sequences

As the board input voltage VIN rises, the output voltages V33USB, V25B, V12B and VCARD of the onboard regulators will rise. Power-on initialization starts when the power supplies of the FPGA have risen. Configuration takes a few seconds (depending on the configuration size). After configuration is done, MAX825 keeps RESET active for 140 ms. Pressing SW7 initiates reconfiguration of the FPGA by using the SPI-ROM.

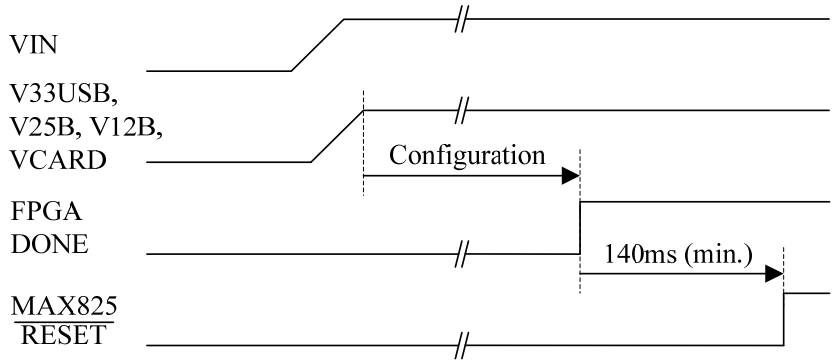

Figure 5 : Power-On Sequences

2.4. Configuration

The JTAG CONFIG connector CN7 is directly connected with the JTAG port of the FPGA. The FPGA connects with the 64-Mbit SPI-ROM through the level shifter. FPGA configuration data is loaded from the SPI-ROM in the Master Serial Mode (SW6-1 = OFF, SW6-2 = ON). The clock frequency of SCK is limited to 10 MHz because of the electrical characteristics of the level shifter. When configuration is successfully done, LED13 turns on.

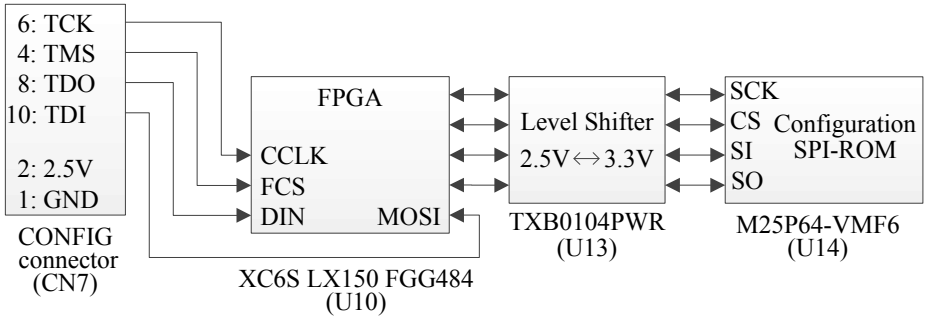

Figure 6 : JTAG Chain

2.5. Clock System

The FPGA clock signal is supplied from the onboard 24.000 MHz oscillator X2 and/or external clock input via the SMA connector J6. The IC Card clock selected by SW2 is supplied from the FPGA or external clock input via the SMA connector J3. When the IC Card clock is supplied from the FPGA, the clock frequency is limited to 4 MHz because of the electrical characteristics of the level shifter.

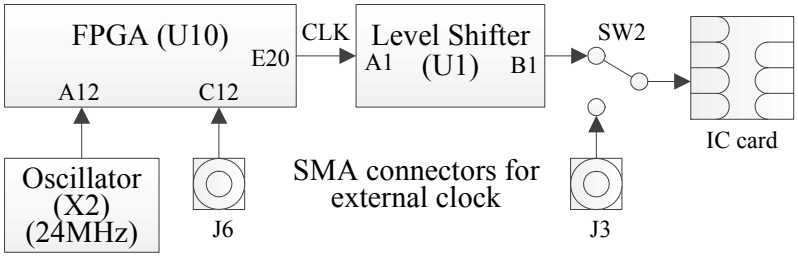

Figure 7 : Clock System

2.6. Measurement Points

The SASEBO-W has a few measurement points consisting of current-sense resistors and SMA connectors. The outer shell (shielding) of each SMA connector is connected to the common ground.

When measuring the high-side current of the IC Card, the low-side current-sense resistor R8 should be bypassed using JP5. The current through the resistor R1 is calculated from the voltage difference between J7 and J1. When measuring the low-side current of the IC Card, the high-side current-sense resistor R1 should be bypassed using JP1. The current through the resistor R8 is calculated from the voltage of J2. When measuring the high-side current of the FPGA, the current is calculated from the voltage difference between J5 and J4.

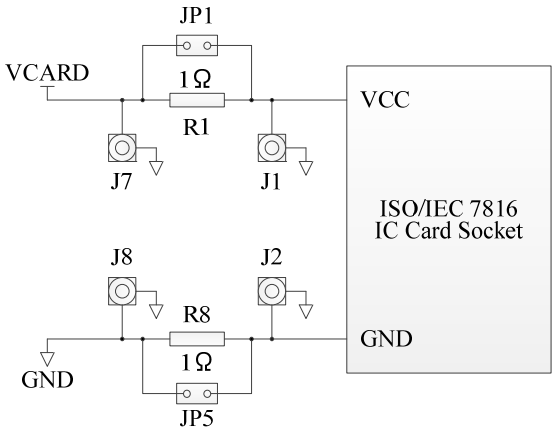

Figure 8 : Measurement Points of IC Card

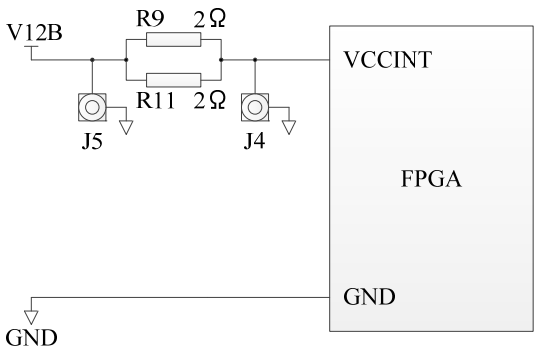

Figure 9 : Measurement Points of FPGA

Table 3 : Measurement Points

Measurement point	Current-sense resistor	Jumper	Supply side	Target side
High side of IC Card	R1 (1 Ω)	JP1	J7	J1
Low side of IC Card	R8 (1 Ω)	JP5	J8	J2
High side of FPGA core	R9 + R11 (1 Ω)	—	J5	J4

2.7. Connectors

Table 4 : SASEBO-W Connectors

Reference Designator	Function
CN1	IC Card external power input
CN2	IC Card connector
CN3	Power output
CN4	FT2232H JTAG (Host)
CN5	USB
CN6	FPGA I/O
CN7	FPGA JTAG (Target)
CN8	SASEBO-W external power input
J1	High-side current-sense resistor of IC Card (IC Card side)
J2	Low-side current-sense resistor of IC Card (IC Card side)
J3	IC Card external clock input
J4	High-side current-sense resistor of FPGA core (FPGA side)
J5	High-side current-sense resistor of FPGA core (Power supply side)
J6	FPGA external clock input
J7	High-side current-sense resistor of IC Card (Power supply side)
J8	Low-side current-sense resistor of IC Card (Power supply side)

Table 5 : CN1 IC Card External Power Input

Pin	Function
1 (▲)	VCARD
2	GND

Table 6 : CN2 IC Card Connector

Pin	Contact	Function
1	C1	VCC
2	C2	RST
3	C3	CLK
4	C4	AUX1
5	C5	GND
6	C6	VPP
7	C7	I/O
8	C8	AUX2

Table 7 : CN3 Power Output

Pin	Function
1	GND
2	5.0 V (VIN)
3	GND
4	5.0 V (VIN)
5	GND
6	N.C.
7	GND
8	2.5 V (V25B)
9	GND
10	2.5 V (V25B)

Table 8 : CN4 FT2232H JTAG (Host)

Pin	Function
1	GND
2	N.C.
3	GND
4	TMS (BDBUS3)
5	GND
6	TCK (BDBUS0)
7	GND
8	TDO (BDBUS2)
9	GND
10	TDI (BDBUS1)
11	GND
12	N.C.
13	GND
14	N.C.

Table 9 : CN5 USB (Device)

Pin	Function
1	VBUS
2	D-
3	D+
4	GND

Table 10 : CN6 FPGA I/O

Pin	Function
1	2.5 V (V25B)
2	2.5 V (V25B)
3	GND
4	GND
5 ~ 36	IOA0 ~ IOB31
37	GND
38	GND
39	2.5 V (V25B)
40	2.5 V (V25B)
41	2.5 V (V25B)
42	2.5 V (V25B)
43	GND
44	GND
45 ~ 76	IOB0 ~ IOB31
77	GND
78	GND
79	2.5 V (V25B)
80	2.5 V (V25B)

Table 11 : CN7 FPGA JTAG (Target)

Pin	Function
1	GND
2	2.5V (V25B)
3	GND
4	TMS (C18)
5	GND
6	TCK (G15)
7	GND
8	TDO (A19)
9	GND
10	TDI (E18)
11	GND
12	N.C.
13	GND
14	N.C.

Table 12 : CN8 SASEBO-W External Power Input

Pin	Function
1 (▲)	VIN
2	GND

Table 13 : J1 High-Side Current-Sense Resistor of IC Card (IC Card Side)

Pin	Function
Center	High-side current-sense resistor of IC Card (IC Card side)
Shield	GND

Table 14 : J2 Low-Side Current-Sense Resistor of IC Card (IC Card Side)

Pin	Function
Center	Low-side current-sense resistor of IC Card (IC Card side)
Shield	GND

Table 15 : J3 IC Card External Clock Input

Pin	Function
Center	IC Card external clock input
Shield	GND

Table 16 : J4 High-Side Current-Sense Resistor of FPGA Core (FPGA Side)

Pin	Function
Center	High-side current-sense resistor of FPGA core (FPGA side)
Shield	GND

Table 17 : J5 High-Side Current-Sense Resistor of FPGA Core (Power Supply Side)

Pin	Function
Center	High-side current-sense resistor of FPGA core (Power supply side)
Shield	GND

Table 18 : J6 FPGA External Clock Input

Pin	Function
Center	FPGA external clock input
Shield	GND

Table 19 : J7 High-Side Current-Sense Resistor of IC Card (Power Supply Side)

Pin	Function
Center	High-side current-sense resistor of IC Card (Power supply side)
Shield	GND

Table 20 : J8 Low-Side Current-Sense Resistor of IC Card (Power Supply Side)

Pin	Function
Center	Low-side current-sense resistor of IC Card (Power supply side)
Shield	GND

2.8. Jumpers

Table 21 : Jumpers

Designator	Functions	Default Settings
JP1	Bypass the high-side current-sense resistor of IC Card	Short (Bypass)
JP2	Select voltage of the onboard regulator	Short only "+3.0 V" (+3.0 V)
JP3	Enable onboard regulator	Short (Enable)
JP4	IC Card power	Open
JP5	Bypass the low-side current-sense resistor of IC Card	Open (Enable)
JP6	FPGA core power	Open
JP7	Connect USB shield ground and signal ground	Short (Connect)
JP8	Enable external reset of FT2232H	Open (Disable)

JP2 must be shorted for just one voltage setting.

Table 22 : JP2 Settings for Voltage Selection of Onboard Regulator

Voltage	Output voltage of onboard regulator for IC Card
+1.8 V	Setting to +1.8 V
+3.0 V	Setting to +3.0 V.
PROG	Setting by FPGA via digital potentiometer. The voltage can be set from 1.3 V to VIN - 0.1V.

2.9. Switches

Table 23 : Switches

Designator	Function
SW1	IC Card power supply setting
SW2	IC Card clock supply setting
SW3	General purpose DIP switch
SW4	General purpose DIP switch
SW5	General purpose push button
SW6	FPGA mode settings
SW7	FPGA reconfiguration
SW8	SASEBO-W power supply setting

Table 24 : SW1　Power Supply Setting of the IC Card

Setting	Function
INT (Default)	IC Card is powered from onboard regulator.
EXT	IC Card is powered from external input (CN1).

Table 25 : SW2　Clock Supply Setting of the IC Card

Setting	Function
R18 side (Default)	IC Card clock is supplied by FPGA.
TP5 side	IC Card clock is supplied via SMA externally (J3).

Table 26 : SW3　FPGA Mode Settings

Switch	Setting	Function
1	OFF (Default)	M0 = High
1	ON	M0 = Low
2	OFF	M1 = High
2	ON (Default)	M1 = Low
3	OFF	SUSPEND = High
3	ON (Default)	SUSPEND = Low
4	OFF	HSWAPEN = High
4	ON (Default)	HSWAPEN = Low

Table 27 : SW8　Power Supply Setting of the SASEBO-W

Setting	Function
USB (Default)	SASEBO-W is powered from the USB bus (CN5).
EXT	SASEBO-W is powered from external input (CN8).

2.10. USB Device Interface

Table 28 : USB Interface Signals

Signal Name	CN5	U8	U9,U10,CN4
USBDM	2 pin	7 pin	-
USBDP	3 pin	8 pin	-
USB ADBUS0	-	16pin	U10.C5
USB ADBUS1	-	17pin	U10.A5
USB ADBUS2	-	18pin	U10.D6
USB ADBUS3	-	19pin	U10.C6
USB ADBUS4	-	21pin	U10.B6
USB ADBUS5	-	22pin	U10.A6
USB ADBUS6	-	23pin	U10.C7
USB ADBUS7	-	24pin	U10.A7
USB ACBUS0	-	26pin	U10.B8
USB ACBUS1	-	27pin	U10.A8
USB ACBUS2	-	28pin	U10.D9
USB ACBUS3	-	29pin	U10.C8
USB ACBUS4	-	30pin	U10.C9
USB ACBUS5	-	32pin	U10.D7
USB ACBUS6	-	33pin	U10.D8
USB ACBUS7	-	34pin	U10.D10
EECS	-	63pin	U9.1
EECLK	-	62pin	U9.2
EEDATA	-	61pin	U9.3,U9.4
FT2232-TCK	-	38pin	CN4.6
FT2232-TDI	-	39pin	CN4.10
FT2232-TDO	-	40pin	CN4.8
FT2232-TMS	-	41pin	CN4.4
FT2232-GPIOH0	-	48pin	-
FT2232-GPIOH1	-	52pin	-
FT2232-GPIOH2	-	53pin	-
FT2232-GPIOH3	-	54pin	-
FT2232-GPIOH4	-	55pin	-
FT2232-GPIOH5	-	57pin	-
FT2232-GPIOH6	-	58pin	-
FT2232-GPIOH7	-	59pin	-
FT2232-GPIOL0	-	43pin	-
FT2232-GPIOL1	-	44pin	-
FT2232-GPIOL2	-	45pin	-
FT2232-GPIOL3	-	46pin	-

3. Examples of settings

The default settings and detail of the switches and jumpers are shown in the previous chapter.

3.1. USB bus power, Low-side measurement of IC Card

Table 29 : USB Bus Power, Low-Side Measurement of IC Card

Designator	Setting	Description
SW8	USB	SASEBO-W is powered from the USB bus.
SW1	INT	IC Card is powered from onboard regulator.
JP2	Short "+3.0 V"	Output voltage of the regulator is +3.0 V.
SW2	R18 side	IC Card clock is supplied by FPGA.
JP1	Short	Bypass high-side current-sense resistor of IC Card.
JP5	Open	Use low-side current sense resistor of IC Card.
J2	Connect to oscilloscope	Measure the low-side current of IC Card.

The other settings are set to default.

3.2. USB bus power, High-side measurement of IC Card

Table 30 : USB Bus Power, High-Side Measurement of IC Card

Designator	Setting	Description
SW8	USB	SASEBO-W is powered from the USB bus.
SW1	INT	IC Card is powered from onboard regulator.
JP2	Short "+3.0 V"	Output voltage of the regulator is +3.0 V.
SW2	R18 side	IC Card clock is supplied by FPGA.
JP1	Open	Use high-side current-sense resistor of IC Card.
JP5	Short	Bypass low-side current-sense resistor of IC Card.
J7	Connect to oscilloscope	Measure the high-side current of IC Card (J7-J1 differential)
J1	Connect to oscilloscope	Measure the high-side current of IC Card (J7-J1 differential)

The other settings are set to default.

3.3. External power input for IC Card, Low-side measurement of IC Card

Table 31 : External Power Input for IC Card, Low-Side Measurement of IC Card

Designator	Setting	Description
SW8	USB	SASEBO-W is powered from the USB bus.
SW1	EXT	IC Card is powered from external input (CN1).
CN1	Connect to power supply	Supply IC Card power
JP2	Short "+3.0 V"	Output voltage of the regulator is +3.0 V.
SW2	R18 side	IC Card clock is supplied by FPGA.
JP1	Short	Bypass high-side current-sense resistor of IC Card.
JP5	Open	Use low-side current sense resistor of IC Card.
J2	Connect to oscilloscope	Measure the low-side current of IC Card.

The other settings are set to default.

4. I/O Assignments

4.1. FPGA

Table 32 : FPGA Configuration and Monitor Signals

Signal Name	Pin	Direction	Destination
CLK	A12	I	X2.3
EXTCLK	C12	I	J6
TCK	G15	--	CN7.6
TDI	E18	--	CN7.10
TDO	A19	--	CN7.8
TMS	C18	--	CN7.4
M0	AA22	I	SW6
M1	U15	I	SW6
SUSPEN	N15	I	SW6
HSWAPEN	A3	I	SW6
PROGRAM	AA1	I	SW7
MISO1	AA20	I	U13.2
CS_B	Y20	O	U13.5
CCLK	Y21	O	U13.4
MSIO0	AB20	O	U13.3
DONE	Y22	O	CONFIG
POWER_OK	C15	I	MAX8902
POWER_OFF	A15	O	MAX8902
SCL	D14	O	ISL95810
SDA	C14	O	ISL95810
LED5	AB19	I	LED
LED6	AA16	I	LED
LED7	AA18	I	LED
LED8	AB16	I	LED
LED9	AB18	I	LED
LED10	AB15	I	LED
LED11	AB17	I	LED
LED12	AA14	I	LED
SW0	R20	I	SW3
SW1	R22	I	SW3
SW2	T21	I	SW3
SW3	T22	I	SW3
SW4	U20	I	SW4
SW5	U22	I	SW4
SW6	V21	I	SW4
SW7	V22	I	SW4
SW8	M19	I	SW5

Table 33 : FPGA - IC Card Interface

Signal Name	Pin	Direction	Destination
CLK	E20	O	IC CARD
RST	C22	O	IC CARD
OE	F18	O	IC CARD
AUX1	H18	IO	IC CARD
AUX2	H19	IO	IC CARD
CARD	D15	I	IC CARD
IO	F20	IO	IC CARD

Table 34 : FPGA GPIO

Signal Name	Pin	Direction	Destination
IOA0	AA10	IO	CN6.5
IOA1	AB10	IO	CN6.6
IOA2	AB9	IO	CN6.7
IOA3	AA8	IO	CN6.8
IOA4	AB8	IO	CN6.9
IOA5	AB7	IO	CN6.10
IOA6	AA6	IO	CN6.11
IOA7	AB6	IO	CN6.12
IOA8	AA4	IO	CN6.13
IOA9	AB4	IO	CN6.14
IOA10	AB3	IO	CN6.15
IOA11	Y7	IO	CN6.16
IOA12	AA2	IO	CN6.17
IOA13	Y3	IO	CN6.18
IOA14	AB2	IO	CN6.19
IOA15	W4	IO	CN6.20
IOA16	Y2	IO	CN6.21
IOA17	Y4	IO	CN6.22
IOA18	Y1	IO	CN6.23
IOA19	U6	IO	CN6.24
IOA20	W3	IO	CN6.25
IOA21	V5	IO	CN6.26
IOA22	W1	IO	CN6.27
IOA23	U3	IO	CN6.28
IOA24	V1	IO	CN6.29
IOA25	T6	IO	CN6.30
IOA26	U1	IO	CN6.31
IOA27	T5	IO	CN6.32
IOA28	P8	IO	CN6.33
IOA29	P7	IO	CN6.34
IOA30	M5	IO	CN6.35
IOA31	M4	IO	CN6.36
IOB0	T2	IO	CN6.45
IOB1	T1	IO	CN6.46
IOB2	R3	IO	CN6.47
IOB3	R1	IO	CN6.48
IOB4	P2	IO	CN6.49
IOB5	P1	IO	CN6.50

IOB6	N3	IO	CN6.51
IOB7	N1	IO	CN6.52
IOB8	M2	IO	CN6.53
IOB9	M1	IO	CN6.54
IOB10	L3	IO	CN6.55
IOB11	L1	IO	CN6.56
IOB12	K2	IO	CN6.57
IOB13	K1	IO	CN6.58
IOB14	J3	IO	CN6.59
IOB15	J1	IO	CN6.60
IOB16	H2	IO	CN6.61
IOB17	H1	IO	CN6.62
IOB18	G3	IO	CN6.63
IOB19	G1	IO	CN6.64
IOB20	F2	IO	CN6.65
IOB21	F1	IO	CN6.66
IOB22	E3	IO	CN6.67
IOB23	E1	IO	CN6.68
IOB24	D2	IO	CN6.69
IOB25	D1	IO	CN6.70
IOB26	C3	IO	CN6.71
IOB27	C1	IO	CN6.72
IOB28	B2	IO	CN6.73
IOB29	B1	IO	CN6.74
IOB30	A2	IO	CN6.75
IOB31	B3	IO	CN6.76

Table 35 : FPGA - USB Interface

Signal Name	Pin	Direction	Destination
USBBDBUS0	C5	IO	U8.16
USBBDBUS1	A5	IO	U8.17
USBBDBUS2	D6	IO	U8.18
USBBDBUS3	C6	IO	U8.19
USBBDBUS4	B6	IO	U8.21
USBBDBUS5	A6	IO	U8.22
USBBDBUS6	C7	IO	U8.23
USBBDBUS7	A7	IO	U8.24
USBBCBUS0	B8	IO	U8.26
USBBCBUS1	A8	IO	U8.27
USBBCBUS2	D9	IO	U8.28
USBBCBUS3	C8	IO	U8.29
USBBCBUS4	C9	IO	U8.30
USBBCBUS5	D7	IO	U8.32
USBBCBUS6	D8	IO	U8.33
USBBCBUS7	D10	IO	U8.34
USBPWREN	B16	I	U8.60
USBSUSPEND	A16	I	U8.36
USBRESET	C17	O	U8.14

4.2. FT2232H

Table 36 : FT2232H JTAG Host and GPIO

Signal Name	Pin	Direction	Destination
FT2232_TCK	U8.38	I	CN4.6
FT2232_TDI	U8.39	IO	CN4.10
FT2232_TDO	U8.40	IO	CN4.8
FT2232_TMS	U8.41	I	CN4.4
GPIOL0	U8.43	IO	-
GPIOL1	U8.44	IO	-
GPIOL2	U8.45	IO	-
GPIOL3	U8.46	IO	-
GPIOH0	U8.48	IO	-
GPIOH1	U8.52	IO	-
GPIOH2	U8.53	IO	-
GPIOH3	U8.54	IO	-
GPIOH4	U8.55	IO	-
GPIOH5	U8.57	IO	-
GPIOH6	U8.58	IO	-
GPIOH7	U8.59	IO	-

4.3. LED

Table 37 : LED

Signal Name	Pin	Direction	Destination
LED1	-	-	FPGA 1.2 V
LED2	-	-	FPGA 2.5 V
LED3	-	-	USB 5.0 V
LED4	-	-	USB 3.3 V

5. Parts List, Circuit Diagram, and Board Layout

Table 38 : Parts List

Description	Part Number	Maker	Reference Designator	Spec.
C1005	GRM155B11E103KA01D	Murata	C5	0.01u
C1005	GRM155F11E104ZA01D	Murata	C2,C3,C9,C11,C12,C19,C21, C22,C23C24,C26,C28,C29,C31, C32,C34,C35,C37,C38,C40,C43, C55,C83,C84,C86,C88	0.1u
C1005	GRM155B31A474KE14D	Murata	C49,C50,C51,C52,C53,C54,C59, C60,C61,C62,C65,C66,C69,C70, C71,C72,C75,C76,C79,C80,C81, C82	0.47u
C2012	LMK212BJ106KD-T	Taiyo Yuden	C1,C4,C10,C13,C25,C36	10u
C1005	GRM155F10J105ZE01D	Murata	C39	1u
C2012	GRM21BB11A225KA01L	Murata	C16,C18	2.2u
C1005	C1005CH1H270J	TDK	C41,C42	27p
C1608	GRM188B30J475KE18D	Murata	C46,C47,C48,C57,C58,C64,C68, C74,C78,C87,C89	4.7u
C3216	GRM31CB30J476ME18L	Murata	C6,C14,C17	47u
C3225	GRM32EF10J107ZE20L	Murata	C44,C45,C56,C63,C67,C73,C77	100u/6.3V
SP-CON	PCG0J271MCL1GS	Nippon Chemi-con	C7,C15	270u/6.3V
C_POL	EMVK6R3ADA220MD55G	Nippon Chemi-con	C20,C27,C30,C85	22u/6.3V
C_POL	KME10VB470M	Nippon Chemi-con	C33	470u/10V
R1005	RK73H1ETTP132F	KOA	R58	1.3k
R1005	RK73H1ETTP1000D	KOA	R10,R13,R21,R41,R42,R52,R54	100
R1005	RK73H1ETTP1003D	KOA	R5,R6,R7,R19	100k
R1005	RK73H1ETTP1002D	KOA	R16,R18,R20,R44,R65	10k
R1005	RK73H1ETTP1103D	KOA	R23	110k
R1005	RK73H1ETTP123F	KOA	R2,R31	12k
R1005	RK73H1ETTP1500D	KOA	R30,R33,R34,R35,R36,R37, R38,R39,R40,R55	150
R1005	RK73H1ETTP1001D	KOA	R43	1k
R1005	RMC1/16SK-222F	Kamaya Electric	R32	2.2k
R1005	RK73H1ETTP2401D	Susumu	R57,R63,R64	2.4k
R1005	RK73H1ETTP3300D	KOA	R22,R56	330
R1005	RK73H1ETTP4701D	KOA	R62,R66	4.7k
R1005	RK73H1ETTP4703D	KOA	R17	470k
R1005	RR0510R-562-D	Susumu	R3	5.6k
R1005	RK73H1ETTP6192F	KOA	R24	61.9k
R1005	RK73Z1ETTD	KOA	R59,R60,R61	0
R1608	RK73Z1JTTD	KOA	R45,R46,R47,R48,R49,L15,L16	0
R1608	RR0816Q-220-D	Susumu	R50	22
R6331	RK73HW3ATTD1R00F	KOA	R1,R8	1
R6331	RK73HW3ATTD2R00F	KOA	R9,R11	2
Resistor Array (1005X4)	CN1E4KTTD103J	KOA	RA1,RA3,RA4,RA5,RA6,RA7, RA8,RA9,RA10,RA11,RA13	10k
Trimmer	ST-32ETA 1KΩ	Copal	VR1,VR2	1k
Trimmer	ST-32ETA 50KΩ	Copal	VR3,VR4	50k

Description	Part Number	Maker	Reference Designator	Spec.
EMI	NFM21PC105B1C	Murata	EMI2	
EMI	LQM21FN100M70	Murata	L4,L5,L7,L9,L10,L17,L18	
Filter	ACM90V-701-2PL-TL	TDK	L1,L2,L3,L6	
Inductor	B82422A3471K100	KOA	L11,L12,L13,L14,L16	470nH
R3216	RK73Z2BTTD	KOA	L15	
LED	SML-210MTT86	Rohm	LED1,LED2,LED3,LED4,LED5, LED6,LED7,LED8,LED9, LED10,LED11,LED12,LED13	
Oscillator	CX3225SB12000D0GEJZ1	Kyocera	X1	
Oscillator	ASE2-24.000MHz-LC	ABRACON	X2	
FPGA	XC6SLX150FGG484	Xilinx	U10	
IC	MAX3378EEUD+	Maxim	U4	
IC	TXB0104PWR	TI	U13	
Reset IC	MAX825ZEXK+	Maxim	U15	
USB IC	FT2232HL	FTDI	U8	
REG IC	LTM8032	Linear Tech.	U3,U5	
REG IC	LP3875EMP-3.3/NOPB	NS	U6	
REG IC	MAX8902BATA+	Maxim	U1	
EEPROM	AT93C46-10SU-2.7	ATMEL	U9	
FLASH ROM	M25P64-VMF6	ST	U14	
SMA Socket	089-NV98B	Yuetsu Seiki	J1,J2,J3,J4,J5,J6,J7,J8	
SW SLIDE	SS-12SBP2	NKK	SW2	
Test Pin	LC-33-G（Yellow）	MAC8	TP5,TP6,TP7,TP8,TP9,TP10, TP11,TP12,TP13	
SIP Connector	Val		U7	
Transistor	DTC114YE	Rohm	Q1,Q3	
Transistor	DTC143EE	Rohm	Q2	
Poly Switch	nanoSMDC075F-2	Tyco	PS1	
Digital Potentiometer	ISL95810WIU8Z	Intersil	U2	
Connector	A1-80PA-2.54DSA(71)	Hirose	CN6	
Connector	A1-10PA-2.54DSA(71)	Hirose	CN3	
Connector	87832-1420	Molex	CN4,CN7	
Connector	B2B-XH(LF)(SN)	JST Mfg.	CN1,CN8	
IC Card Socket	ID2M-8S-2.54DS(72)	Hirose	CN2	
USB Connector	XM7B-0422	Omron	CN5	
DIP-SW4	A6S-4104	Omron	SW3,SW4,SW6	
Switch	CS-12AAP1	NKK	SW1,SW8	
Switch	B3S-1000	Omron	SW5,SW7	
Jumper Post	B2P-SHF-1AA(LF)(SN)	JST Mfg.	JP4,JP6	
Jumper Post	XG8S-0231	Omron	JP1,JP3,JP5,JP7,JP8	
Jumper Post	XG8S-0631	Omron	JP2	

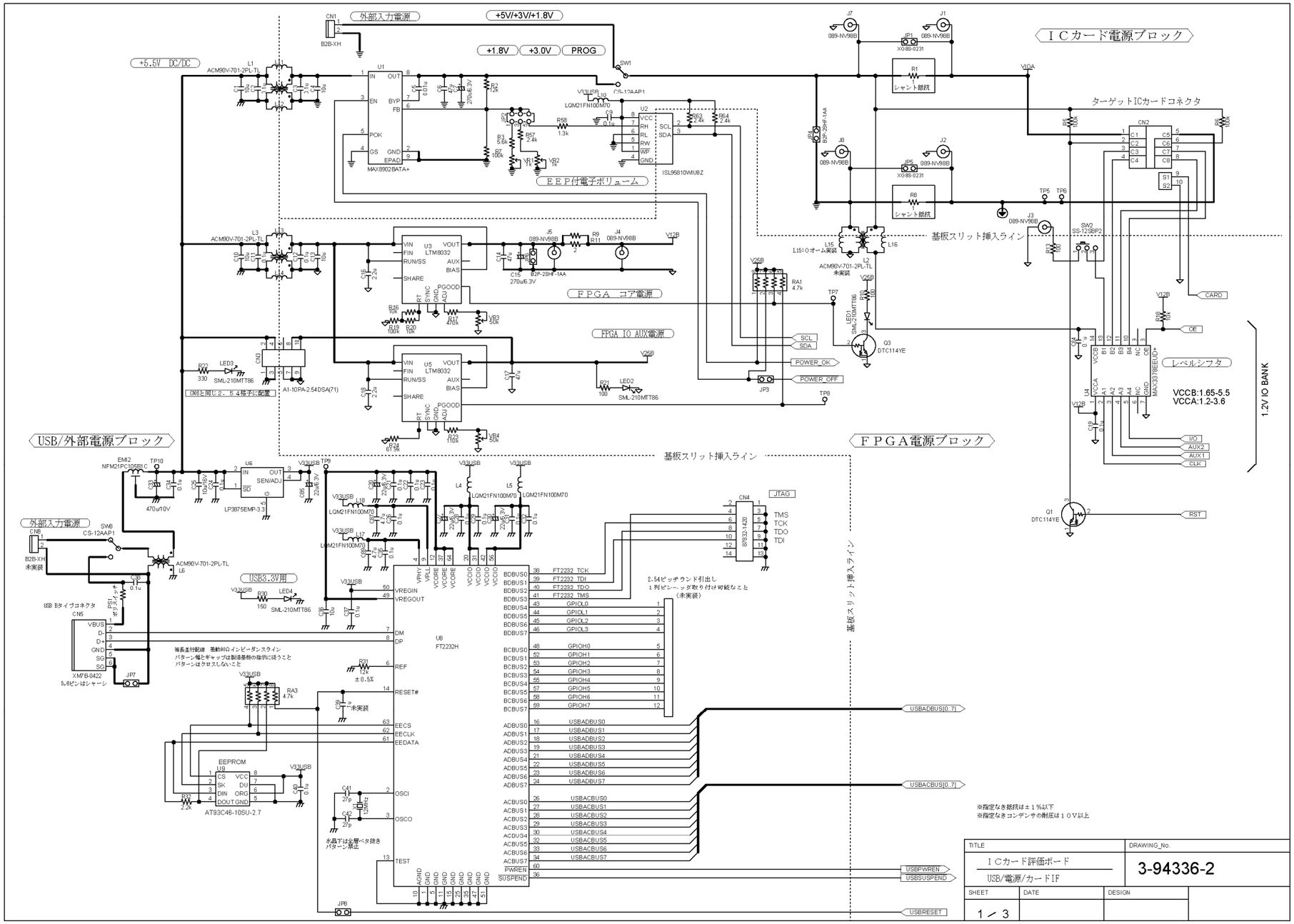

Figure 10 : SASEBO-W FPGA Peripheral Circuit (Power, IC Card, and USB Interface)

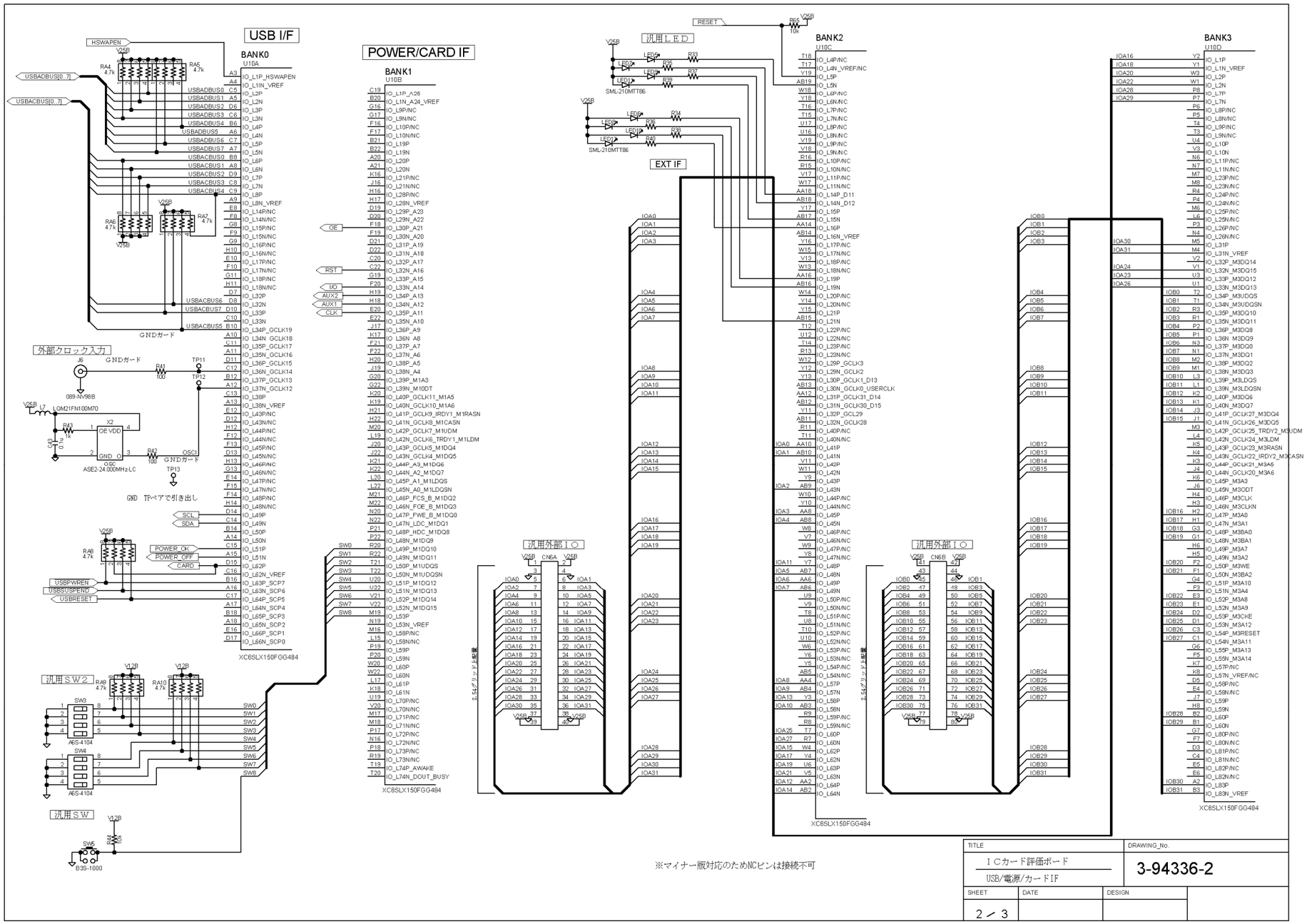

Figure 11：SASEBO-W FPGA Peripheral Circuit (Clock, LED, Switch, and GPIO)

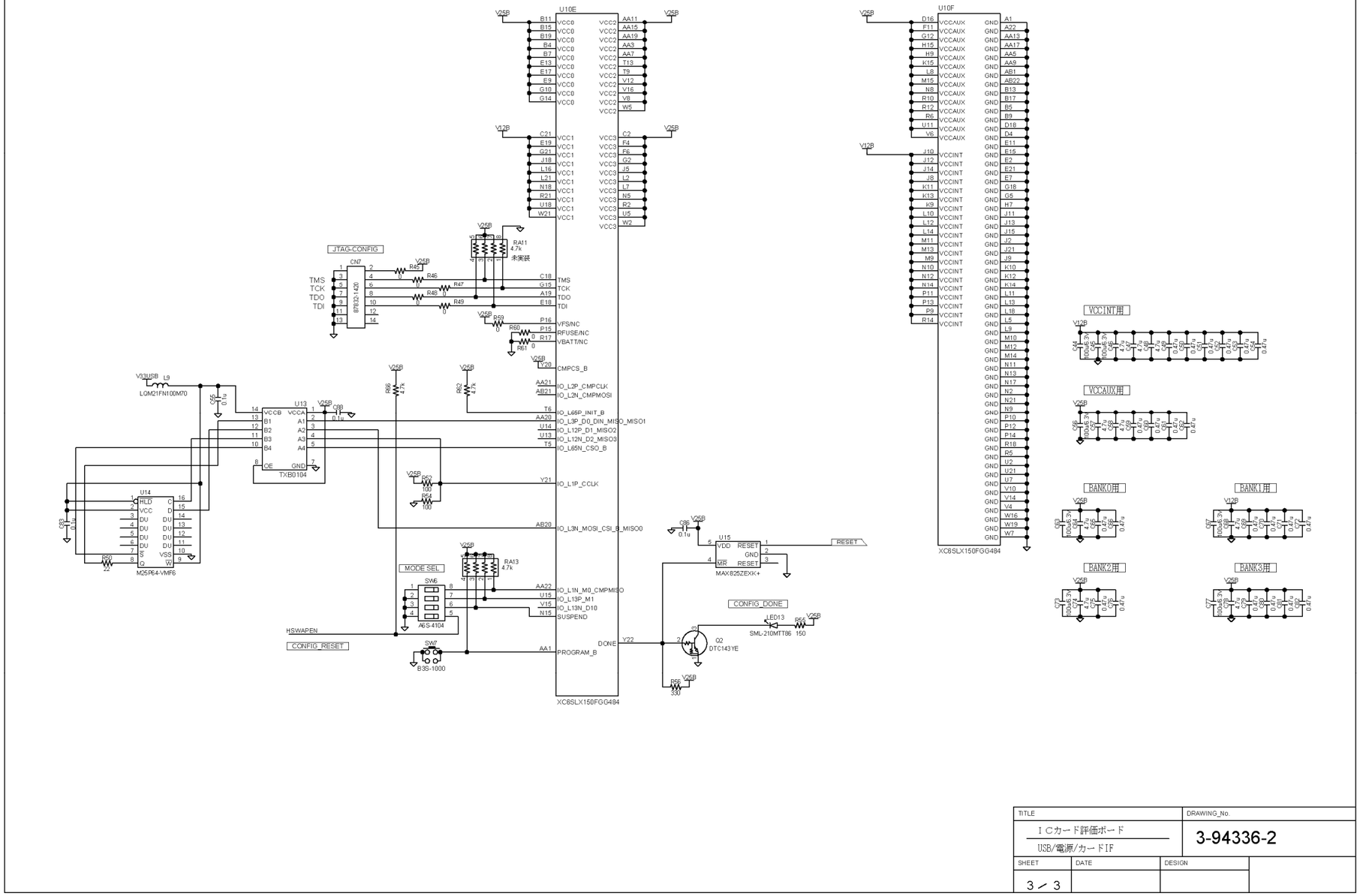

Figure 12 : SASEBO-W FPGA Peripheral Circuit (FPGA Configuration, JTAG and Power)

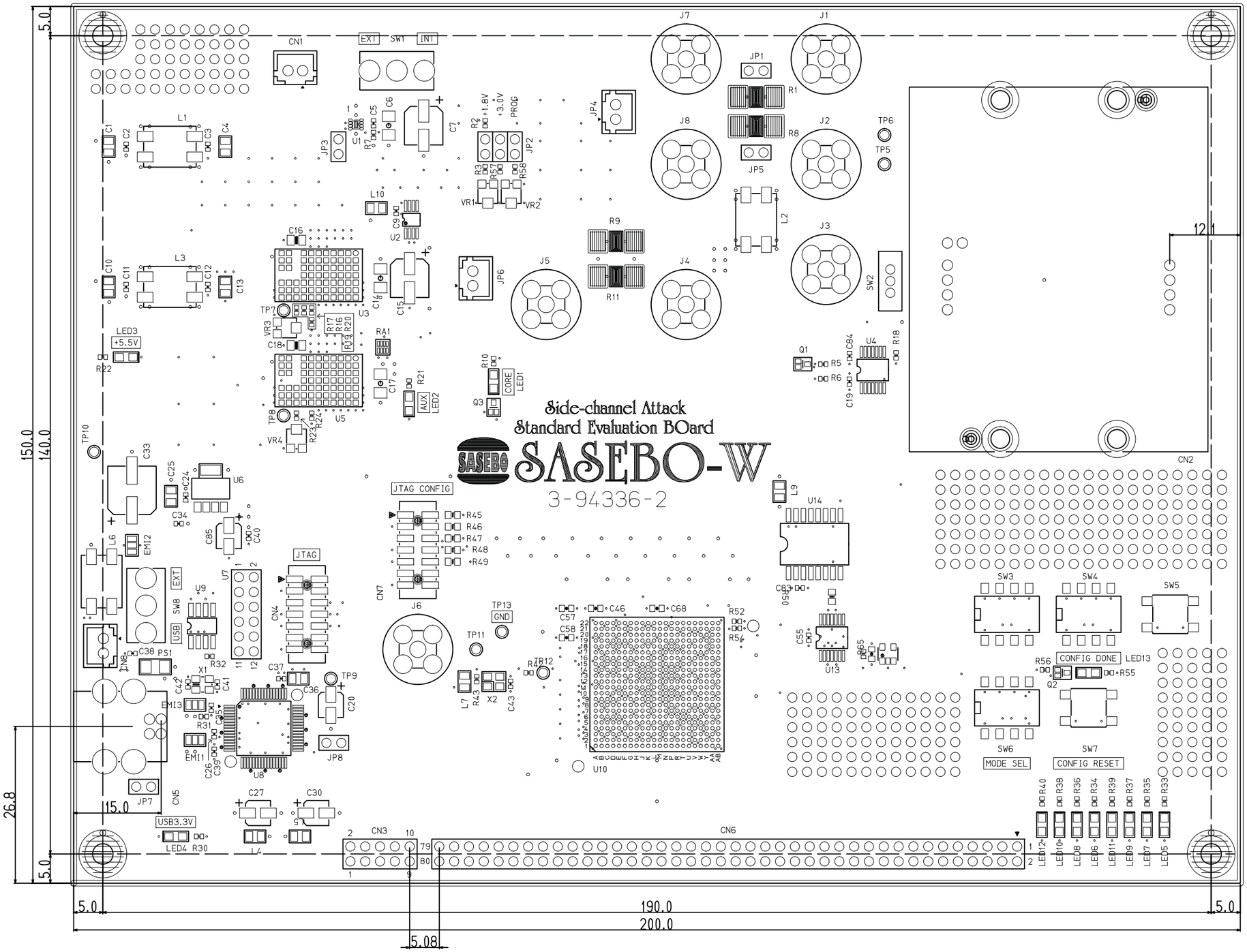

Figure 13 : Part-side Silk Screen / Drawing (Composite)

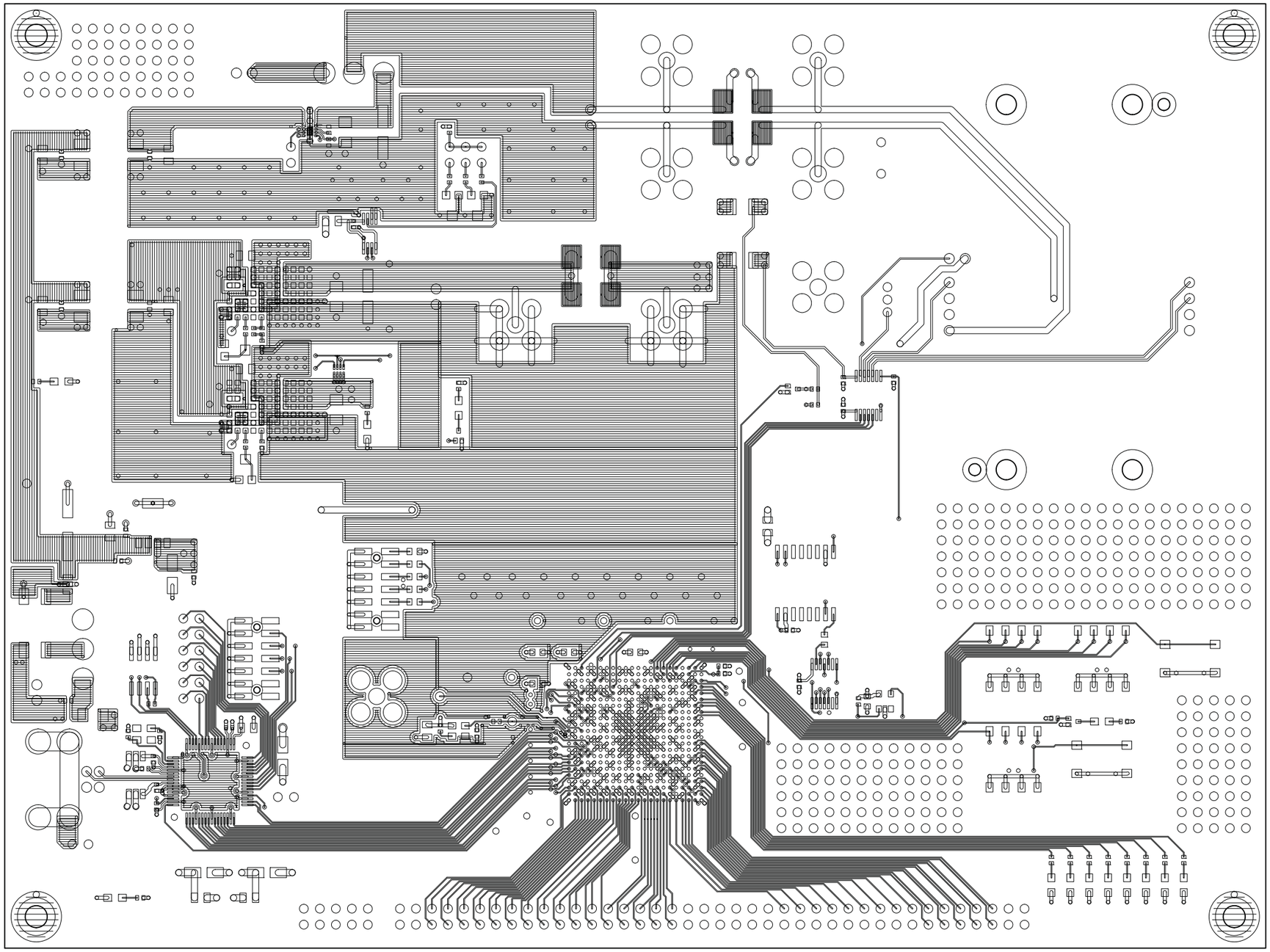

Figure 14 : Layer 1 Pattern

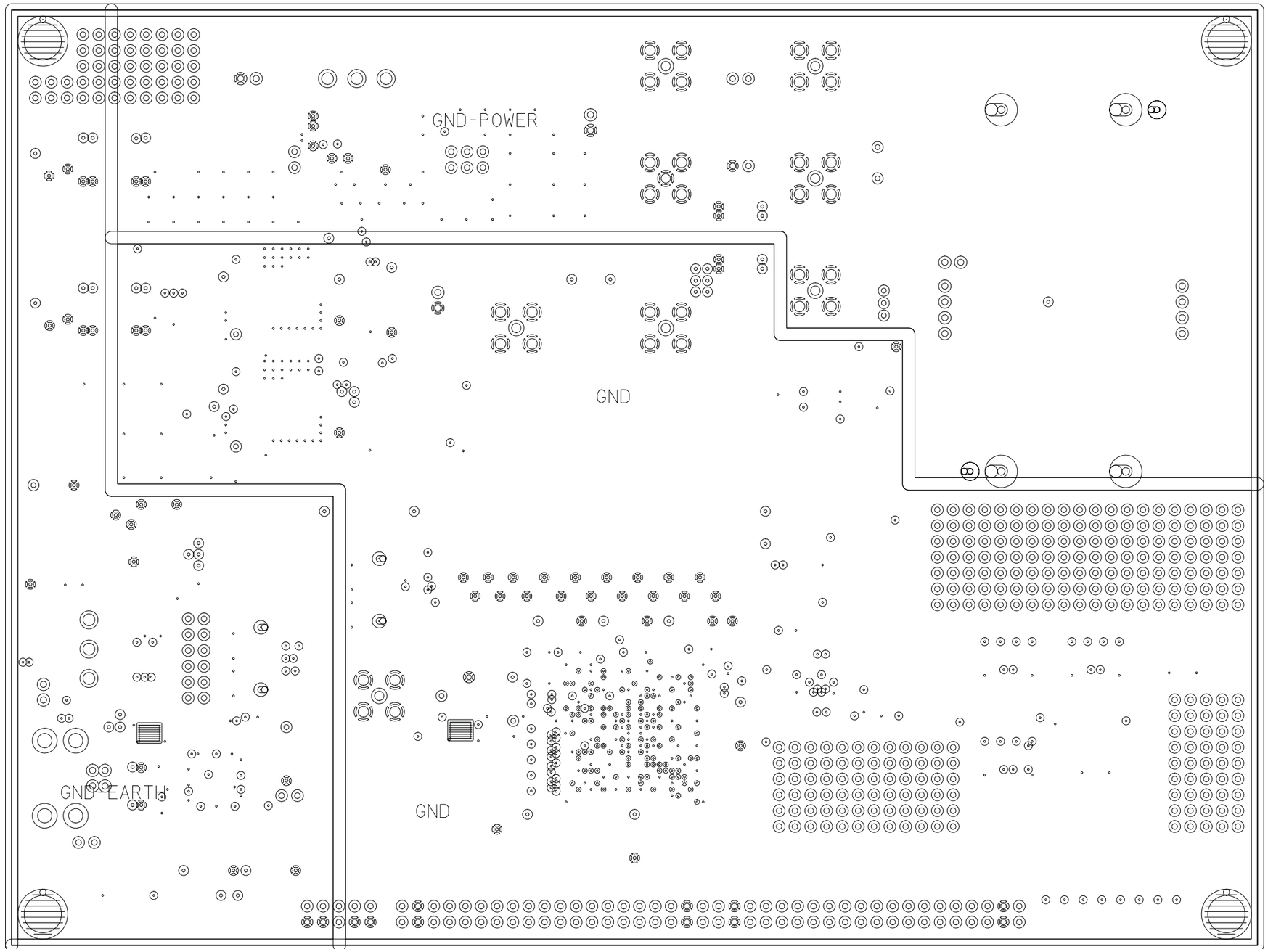

Figure 15 : Layer 2 Pettern (Negative)

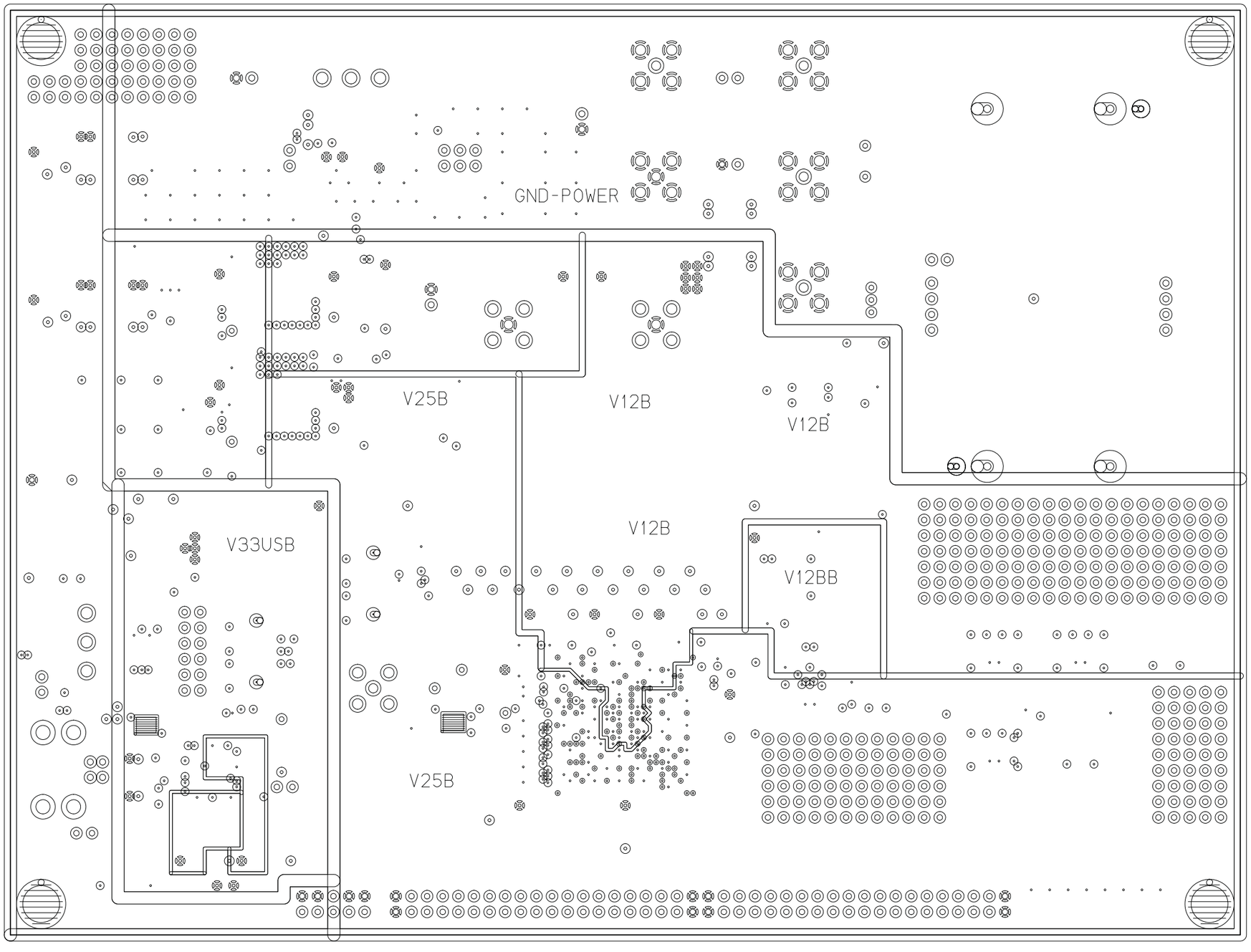

Figure 16 : Layer 3 Pattern (Negative)

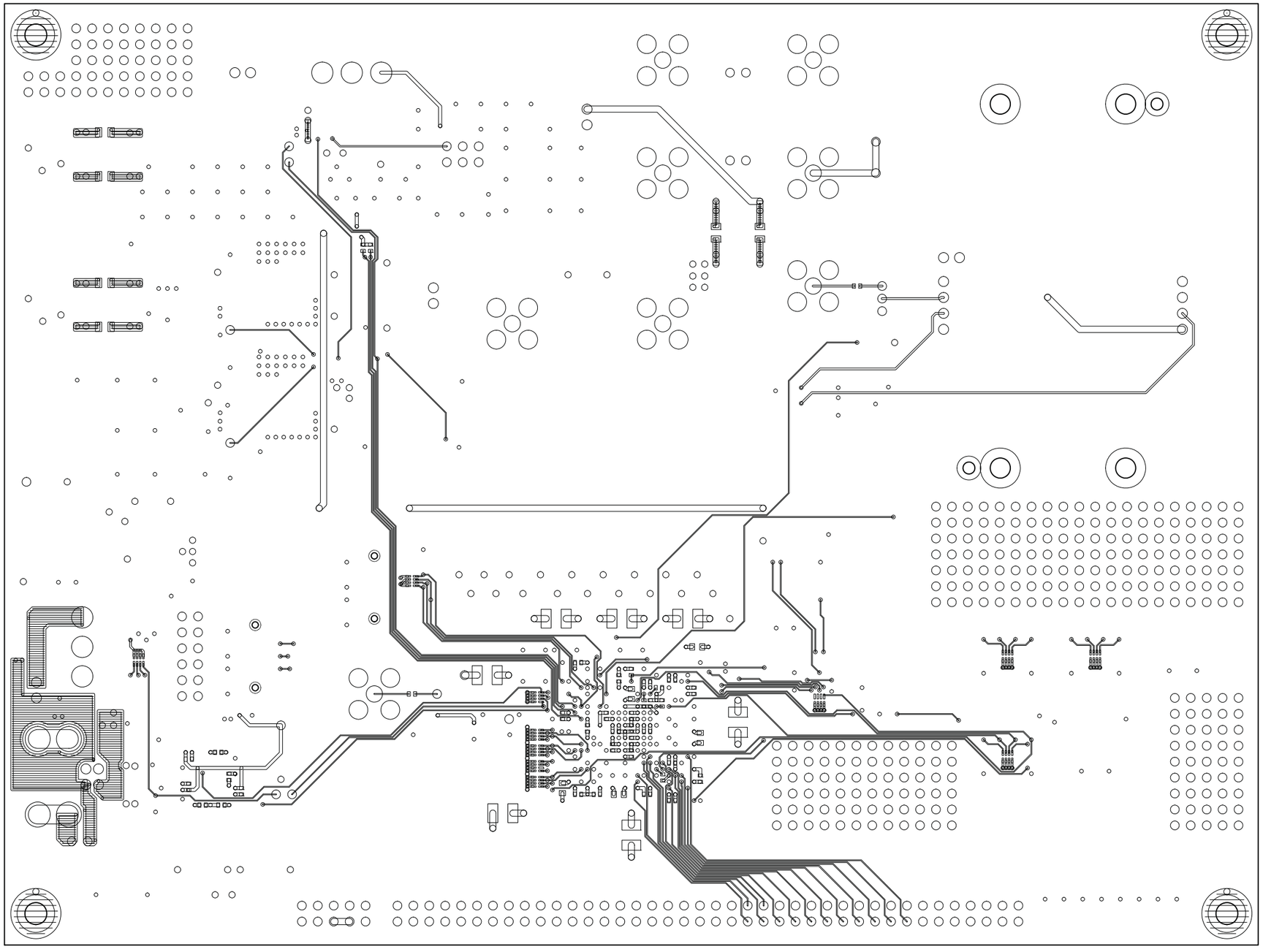

Figure 17 : Layer 4 Patter

The SASEBO-W board was developed by AIST in undertaking projects sponsored by JST (Japan Science and Technology Agency)

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